IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANT(S):	HUH, Hoon et al.	**GROUP ART UNIT:** 2616
APPLICATION NO.:	09/888,915	**EXAMINER:** MOORE, Ian N.
FILING DATE:	June 25, 2001	**DOCKET:** 678-682 (P9821)

FOR: **METHOD AND APPARATUS FOR TRANSMITTING DATA RATE CONTROL INFORMATION IN MOBILE TELECOMMUNICATION SYSTEM FOR PACKET DATA TRANSMISSION**

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Commissioner for Patents
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APPELLANTS' REPLY BRIEF

In response to the Examiner's Answer mailed October 18, 2007, Appellant respectfully submits that based on at least the arguments provided in Appellants' Brief on Appeal of August 6, 2007, Claims 1-21 and 30-39 are patentable over the applied references. The following comments are respectfully submitted in order to address statements made in the Examiner's Answer.

The Examiner raises no new grounds for rejection in the Examiner's Answer.

The allegations raised in the Examiner's Answer do not change the fact that independent Claims 1, 4, 8, 11 and 15 are patentable over Esteves, and that independent Claims 30, 33 and 37 are patentable over Esteves in view of the Proposed High Data Rate (HDR) Standard.

1. A request for data rate control is not and cannot be equated with an indicator that indicates that data rate control has been reliably received

Throughout prosecution, Appellants have maintained that the data rate control (DRC) request indicator (DRI) bit is not and cannot be equated with the balanced state bit of Esteves.

The DRI bit is a request indicating whether or not data rate control (DRC) is required. The DRI bit is a request sent from an Access Network (AN) to a Access Terminal (AT). The DRI bit requests data rate control (DRC) from the AT.

Esteves teaches a balanced state bit. The balanced state bit indicates if a base station is reliably receiving DRC information. The balanced state bit is "sent to the mobile station, thereby indicating to the mobile station that the system is in an unbalanced state such that reverse link is unable to support transmission of the data rate information".[1] "[T]he mobile station will detect an unbalanced condition when operating in the variable rate mode if it receives two consecutive messages from the base station indicating that the base station is unable to receive DRC messages on the reverse link."[2] Therefore, the balanced state bit is used by a mobile station to detect an unbalanced condition. The balanced state bit is ***not*** a request for DRC information.

2. The Examiner mischaracterizes the DRI bit of the claims of the present application

The Examiner states, "it is clear that the appellant's DRI bit (which is set 0 or 1) is used the [sic] access network (i.e. base station) to determine and indicate the reliability of the of the links so that Data Rate Control information can be sent accordingly."[3] This is an incorrect characterization of the DRI bit of the present application. The DRI bit does not "determine and indicate the reliability of the links". The DRI bit indicates if the DRC information is required.[4]

3. The Examiner mischaracterizes the balanced state bit of Esteves

The Examiner states, "it is clear that balanced bit (which is set 0 or 1) is used by the base station to determine and indicate the reliably [sic] of the links so that Data Rate Control information can be sent in response to balanced bit...transmitting the balanced bit...set to 1 implies that

[1] See Esteves at col. 5, lines 30-33.
[2] See Esteves at col. 5, lines 34-38.
[3] See Examiner's Answer at page 16, fifth paragraph.
[4] See e.g. Claims 1, 4, 8, 11 and 15.

whether/if [sic] the DRC information [sic] required." Esteves clearly states that its balanced state bit indicates whether or not a base station is reliably receiving DRC information.[5] This is all that the balanced state bit of Esteves indicates.

4. Esteves does not disclose, "determining...a last time slot of the transmission period"

The Examiner alleges that Esteves discloses determining a last time slot of the transmission period,[6] and in doing so mischaracterizes Esteves. The Examiner alleges that Esteves "monitors and determines each time slot"[7] and cites col 4, lines 37-45 as disclosing such features. Esteves at col. 4, lines 37-45 states:

> In addition, if the base station is able to reliably receive DRC messages from the mobile station on the data rate control channel, the base station sends a balanced state bit (i.e., the bit is set to 0 or 1) to the mobile station indicating that the base station is reliably receiving the DRC messages. The balanced state bit is sent to the mobile station on the forward link periodically and, in the preferred embodiment, the balanced state bit is sent to the mobile station on the forward link once every 400 msec.

Obviously, this section has nothing to do with monitoring and determining time slots. Further, even if it can be reasoned that Esteves discloses monitoring time slots, Esteves is silent as to any determination of a time slot being a last time slot of a transmission period.

5. Esteves and Proposed HDR standard do not disclose, "DRC information is generated in at least one predetermined slot, the at least one predetermined slot being before the last slot and after the packet data and in the first transmission period"

In the present application, a specific position is defined for the transmission of the DRC information. The DRC information is generated in at least one predetermined slot. The at least one predetermined slot being before the last slot and after the packet data and in the first transmission period. At least three conditions are required for the at least one predetermined slot; it must be: (a) before the last slot, (b) after the packet data, and (c) in the first transmission period.

It is respectfully noted that that which is alleged as being disclosed at cited sections of the

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[5] See Esteves at col. 5, lines 27-30.
[6] See Examiner's Answer at page 19, third paragraph.
[7] See Examiner's Answer at page 19, third paragraph.

cited references, is in fact not disclosed at all.[8]

Esteves et al. does not transmit the DRC information between the packet data and the last slot of the first transmission period.

The Proposed HDR Standard in FIG. 9-10 clearly illustrates that start of the DRC is during the packet data, i.e. "pilot/DRC_n" begins transmission during "AN Sending DATA_n" and during "AT receiving DATA_n and PILOT_n".

6. Conclusion

It is well settled that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); and, that "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner has failed to show that each and every element of Claims 1, 4, 8, 11 and 15, and in as complete detail as is contained therein, are taught in or suggested by the prior art. The Examiner has failed to make out a prima facia case for an anticipation rejection.

Based on at least the foregoing, as the Examiner has failed to make out a prima facia case for an anticipation rejection, independent Claims 1, 4, 8, 11 and 15 are not anticipated by Esteves, and therefore, the rejection of Claims 1-21 must be reversed.

It is also well settled that in order for a rejection under 35 U.S.C. §103(a) to be appropriate, the claimed invention must be shown to be obvious in view of the prior art as a whole. A claim may be found to be obvious if it is first shown that all of the recitations of a claim are taught in the prior art or are suggested by the prior art. In re Royka, 490 F.2d 981, 985, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974), cited in M.P.E.P. §2143.03.

The Examiner has failed to show that all of the recitations of Claims 30, 33 and 37 are taught or suggested by the prior art or and combination thereof. Accordingly, the Examiner has failed to

[8] See Examiner's Answer at page 19. The alleged disclosures are not taught or disclosed at the cited locations (nor anywhere else for that matter).

make out a prima facie case for an obviousness rejection.

Based on at least the foregoing, as the Examiner has failed to make out a prima facia case for an obviousness rejection, independent Claims 30, 33 and 37 are not rendered obvious by Esteves in view of Proposed HDR Standard, and therefore, the rejection of Claims 30-39 must be reversed.

Dated: December 18, 2007

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